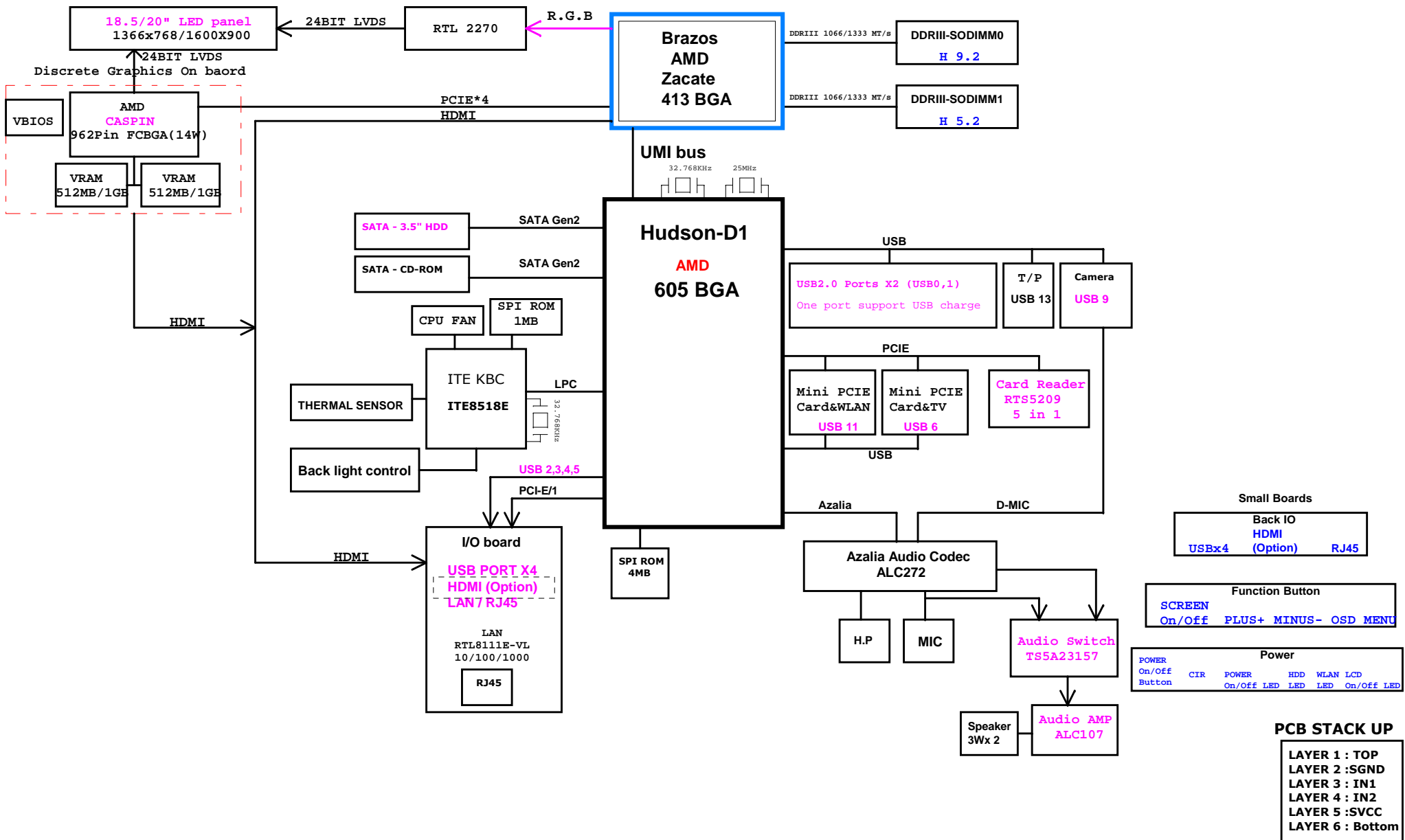


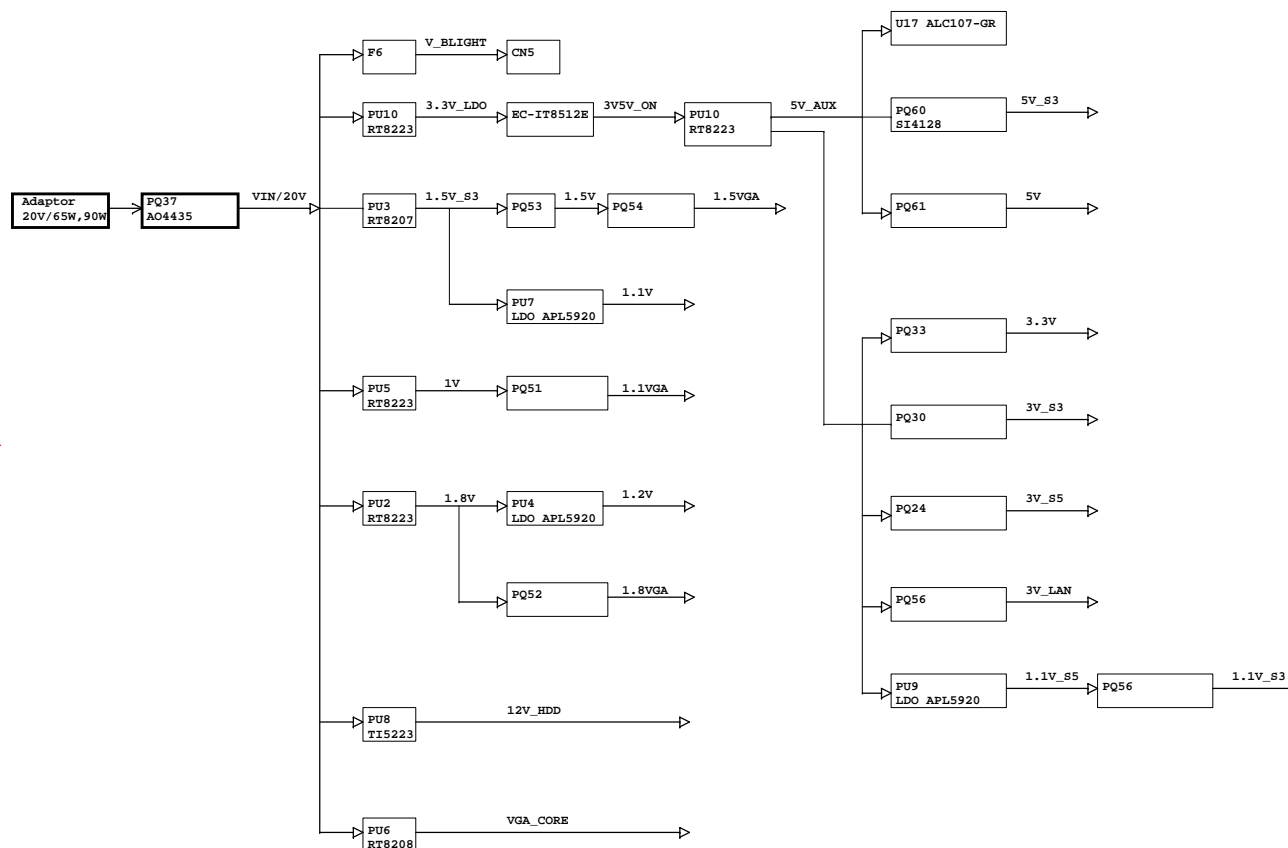
C325/C225 Brazos BLOCK DIAGRAM



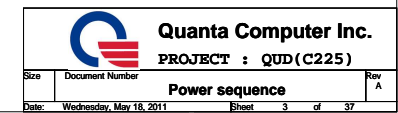
Voltage Rails

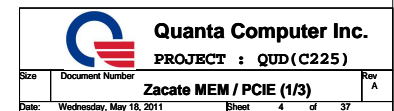
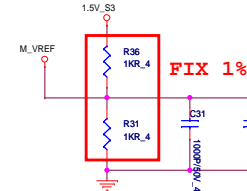
Power	Voltage	S0	S3	S4	S5	G1	On Signal
VCCRTC	3V	ON	ON	ON	ON	ON	Adaptor IN
VIN	20V	ON	ON	ON	ON	OFF	Adaptor IN
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor IN
2V_AUX	3.3V	ON	ON	ON	ON/OFF	OFF	Adaptor IN
3V_S5	3.3V	ON	ON	OFF	OFF	OFF	S5_ON15V
1.1V_S5	1.1V	ON	ON	OFF	OFF	OFF	S5_ON15V
5V_S3	5V	ON	ON	OFF	OFF	OFF	MAINON_10V15
3V_S3	3.3V	ON	ON	OFF	OFF	OFF	MAINON_10V15
1.5V_S3	1.5V	ON	ON	OFF	OFF	OFF	MAINON_10V15
1.1V_S3	1.1V	ON	ON	OFF	OFF	OFF	MAINON_10V15
5V	5V	ON	OFF	OFF	OFF	OFF	MAINON_10
3V	3.3V	ON	OFF	OFF	OFF	OFF	MAINON_10
1.8V	1.8V	ON	OFF	OFF	OFF	OFF	MAINON_10
1.5V	1.5V	ON	OFF	OFF	OFF	OFF	MAINON_20
1.2V	1.2V	ON	OFF	OFF	OFF	OFF	MAINON_20
1.1V	1.1V	ON	OFF	OFF	OFF	OFF	MAINON_20
1V	1.05V	ON	OFF	OFF	OFF	OFF	MAINON_20
BIOS_VFORM	0.75V	ON	OFF	OFF	OFF	OFF	BIOS_V
GPU_CORE	ON	ON	OFF	OFF	OFF	OFF	VFORM
NB_CORE	ON	ON	OFF	OFF	OFF	OFF	VFORM
VGA_CORE	1.8V	ON	OFF	OFF	OFF	OFF	MAINON_2
1.8_VGA	1.8V	ON	OFF	OFF	OFF	OFF	MAINON_20P15
1.5_VGA	1.5V	ON	OFF	OFF	OFF	OFF	MAINON_20P15
1.2_VGA	1V	ON	OFF	OFF	OFF	OFF	MAINON_20P15

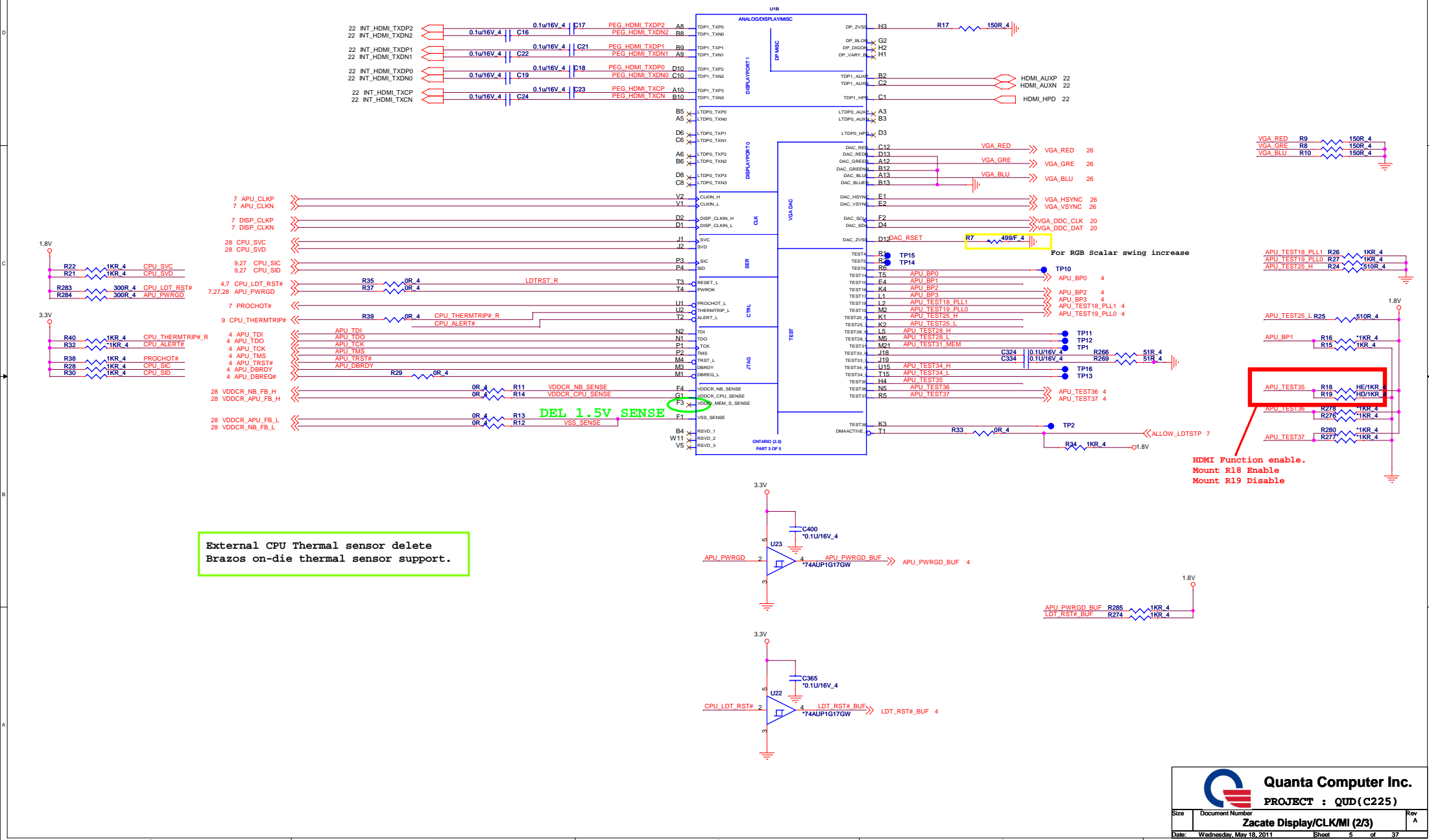
When RTC wake up and S5 WOL Function enable, 3V_S5 will turn on in S5 mode.

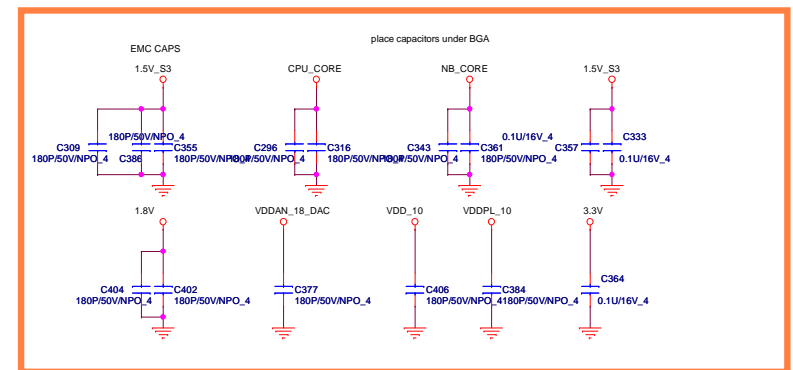
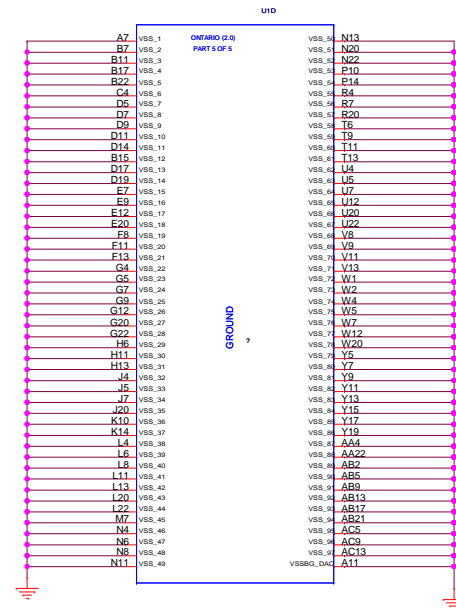


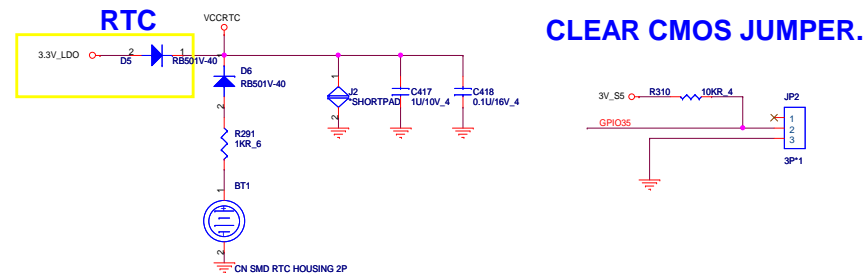
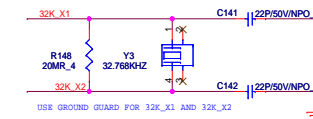
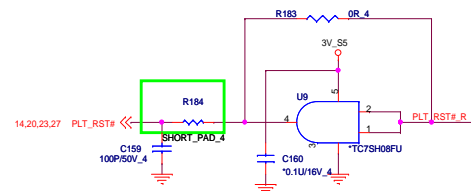
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HDD

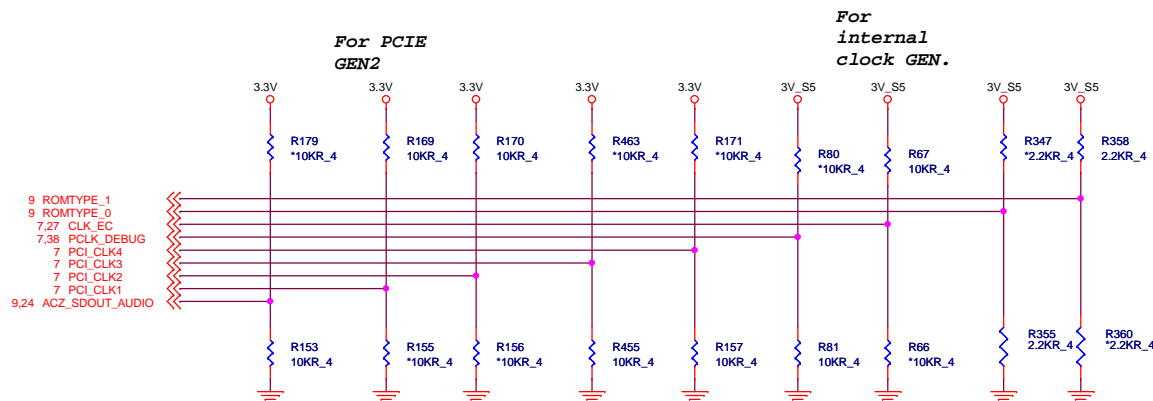




REQUIRED STRAPS



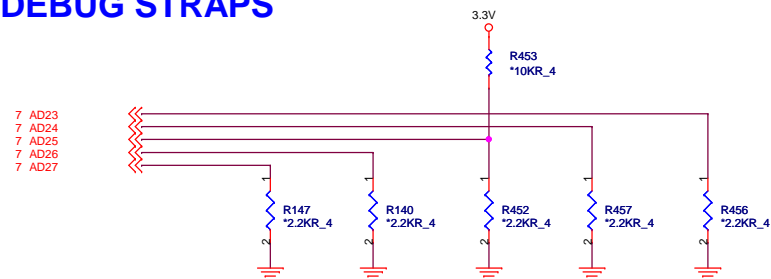
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



	ACZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	INT_EC_EN	INT_CLK_EN	ROMTYPE_1/0
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enable DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK MODE	INTERNAL EC ENABLED	INT. CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM DEFAULT
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disable	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE DEFAULT	INTERNAL EC DISABLED DEFAULT	EXT. CLKGEN ENABLE	L,H=LPC ROM L, L=FWH ROM

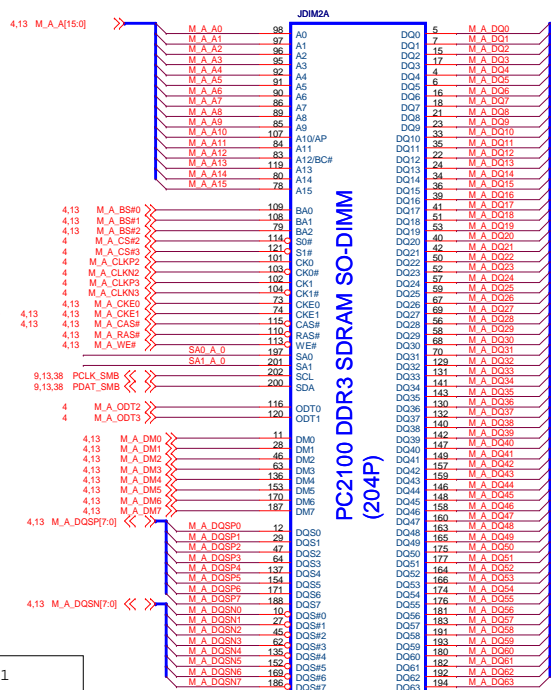
internal have pull Hi 10K

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE I2C ROM DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE I2C ROM use REQ3# as SDA use GNT3# as SCL	ENABLE PCI MEM BOOT

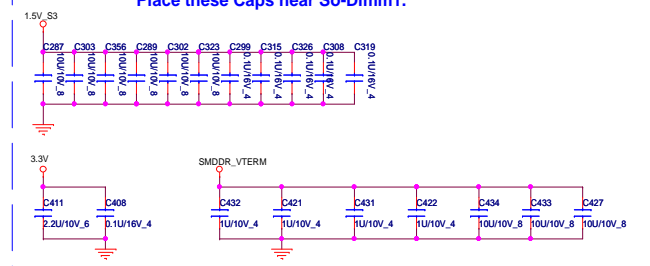
CHANNEL A DIMM 1 H5.2

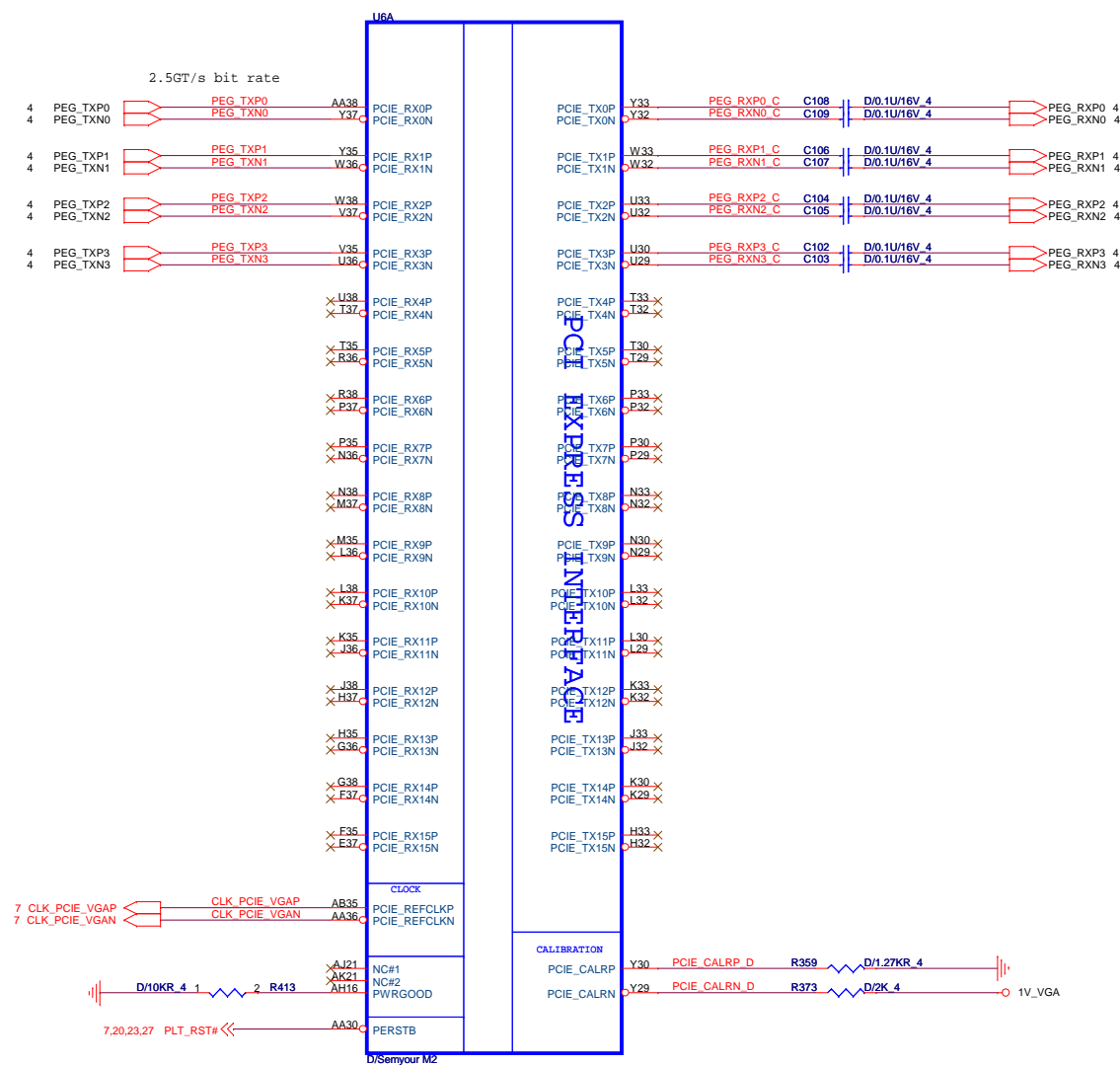


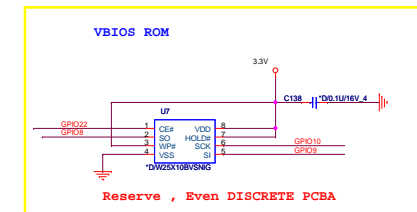
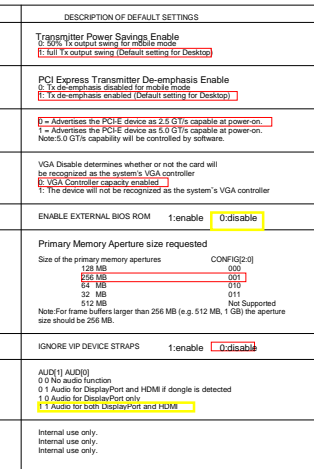
PC2100 DDR3 SDRAM SO-DIMM (204P)

Pin	Signal	Pin	Signal
1	M.A. A0	109	M.A. BSH0
2	M.A. A1	108	M.A. BSH1
3	M.A. A2	107	M.A. BSH2
4	M.A. A3	106	M.A. CS#
5	M.A. A4	105	M.A. CS#
6	M.A. A5	104	M.A. CLK#
7	M.A. A6	103	M.A. CLK#
8	M.A. A7	102	M.A. CLK#
9	M.A. A8	101	M.A. CLK#
10	M.A. A9	100	M.A. CLK#
11	M.A. A10	99	M.A. CKE0
12	M.A. A11	98	M.A. CKE1
13	M.A. A12	97	M.A. CAS#
14	M.A. A13	96	M.A. RAS#
15	M.A. A14	95	M.A. WE#
16	M.A. A15	94	M.A. WE#
17	M.A. A16	93	M.A. WE#
18	M.A. A17	92	M.A. WE#
19	M.A. A18	91	M.A. WE#
20	M.A. A19	90	M.A. WE#
21	M.A. A20	89	M.A. WE#
22	M.A. A21	88	M.A. WE#
23	M.A. A22	87	M.A. WE#
24	M.A. A23	86	M.A. WE#
25	M.A. A24	85	M.A. WE#
26	M.A. A25	84	M.A. WE#
27	M.A. A26	83	M.A. WE#
28	M.A. A27	82	M.A. WE#
29	M.A. A28	81	M.A. WE#
30	M.A. A29	80	M.A. WE#
31	M.A. A30	79	M.A. WE#
32	M.A. A31	78	M.A. WE#
33	M.A. A32	77	M.A. WE#
34	M.A. A33	76	M.A. WE#
35	M.A. A34	75	M.A. WE#
36	M.A. A35	74	M.A. WE#
37	M.A. A36	73	M.A. WE#
38	M.A. A37	72	M.A. WE#
39	M.A. A38	71	M.A. WE#
40	M.A. A39	70	M.A. WE#
41	M.A. A40	69	M.A. WE#
42	M.A. A41	68	M.A. WE#
43	M.A. A42	67	M.A. WE#
44	M.A. A43	66	M.A. WE#
45	M.A. A44	65	M.A. WE#
46	M.A. A45	64	M.A. WE#
47	M.A. A46	63	M.A. WE#
48	M.A. A47	62	M.A. WE#
49	M.A. A48	61	M.A. WE#
50	M.A. A49	60	M.A. WE#
51	M.A. A50	59	M.A. WE#
52	M.A. A51	58	M.A. WE#
53	M.A. A52	57	M.A. WE#
54	M.A. A53	56	M.A. WE#
55	M.A. A54	55	M.A. WE#
56	M.A. A55	54	M.A. WE#
57	M.A. A56	53	M.A. WE#
58	M.A. A57	52	M.A. WE#
59	M.A. A58	51	M.A. WE#
60	M.A. A59	50	M.A. WE#
61	M.A. A60	49	M.A. WE#
62	M.A. A61	48	M.A. WE#
63	M.A. A62	47	M.A. WE#
64	M.A. A63	46	M.A. WE#
65	M.A. A64	45	M.A. WE#
66	M.A. A65	44	M.A. WE#
67	M.A. A66	43	M.A. WE#
68	M.A. A67	42	M.A. WE#
69	M.A. A68	41	M.A. WE#
70	M.A. A69	40	M.A. WE#
71	M.A. A70	39	M.A. WE#
72	M.A. A71	38	M.A. WE#
73	M.A. A72	37	M.A. WE#
74	M.A. A73	36	M.A. WE#
75	M.A. A74	35	M.A. WE#
76	M.A. A75	34	M.A. WE#
77	M.A. A76	33	M.A. WE#
78	M.A. A77	32	M.A. WE#
79	M.A. A78	31	M.A. WE#
80	M.A. A79	30	M.A. WE#
81	M.A. A80	29	M.A. WE#
82	M.A. A81	28	M.A. WE#
83	M.A. A82	27	M.A. WE#
84	M.A. A83	26	M.A. WE#
85	M.A. A84	25	M.A. WE#
86	M.A. A85	24	M.A. WE#
87	M.A. A86	23	M.A. WE#
88	M.A. A87	22	M.A. WE#
89	M.A. A88	21	M.A. WE#
90	M.A. A89	20	M.A. WE#
91	M.A. A90	19	M.A. WE#
92	M.A. A91	18	M.A. WE#
93	M.A. A92	17	M.A. WE#
94	M.A. A93	16	M.A. WE#
95	M.A. A94	15	M.A. WE#
96	M.A. A95	14	M.A. WE#
97	M.A. A96	13	M.A. WE#
98	M.A. A97	12	M.A. WE#
99	M.A. A98	11	M.A. WE#
100	M.A. A99	10	M.A. WE#
101	M.A. A100	9	M.A. WE#
102	M.A. A101	8	M.A. WE#
103	M.A. A102	7	M.A. WE#
104	M.A. A103		

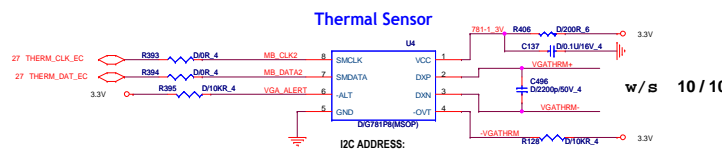
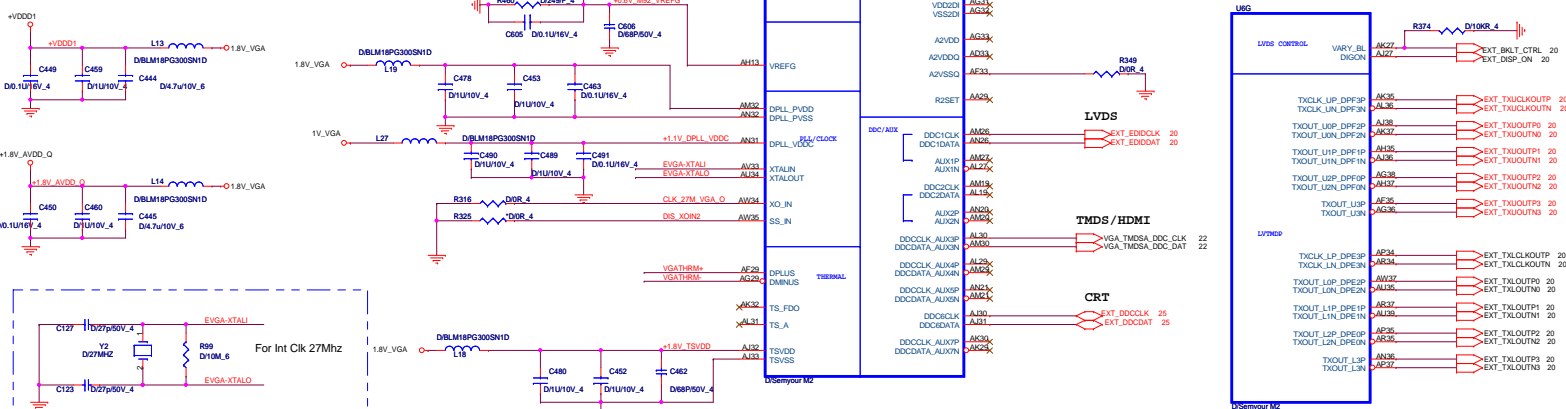
Place these Caps near So-Dimm1.



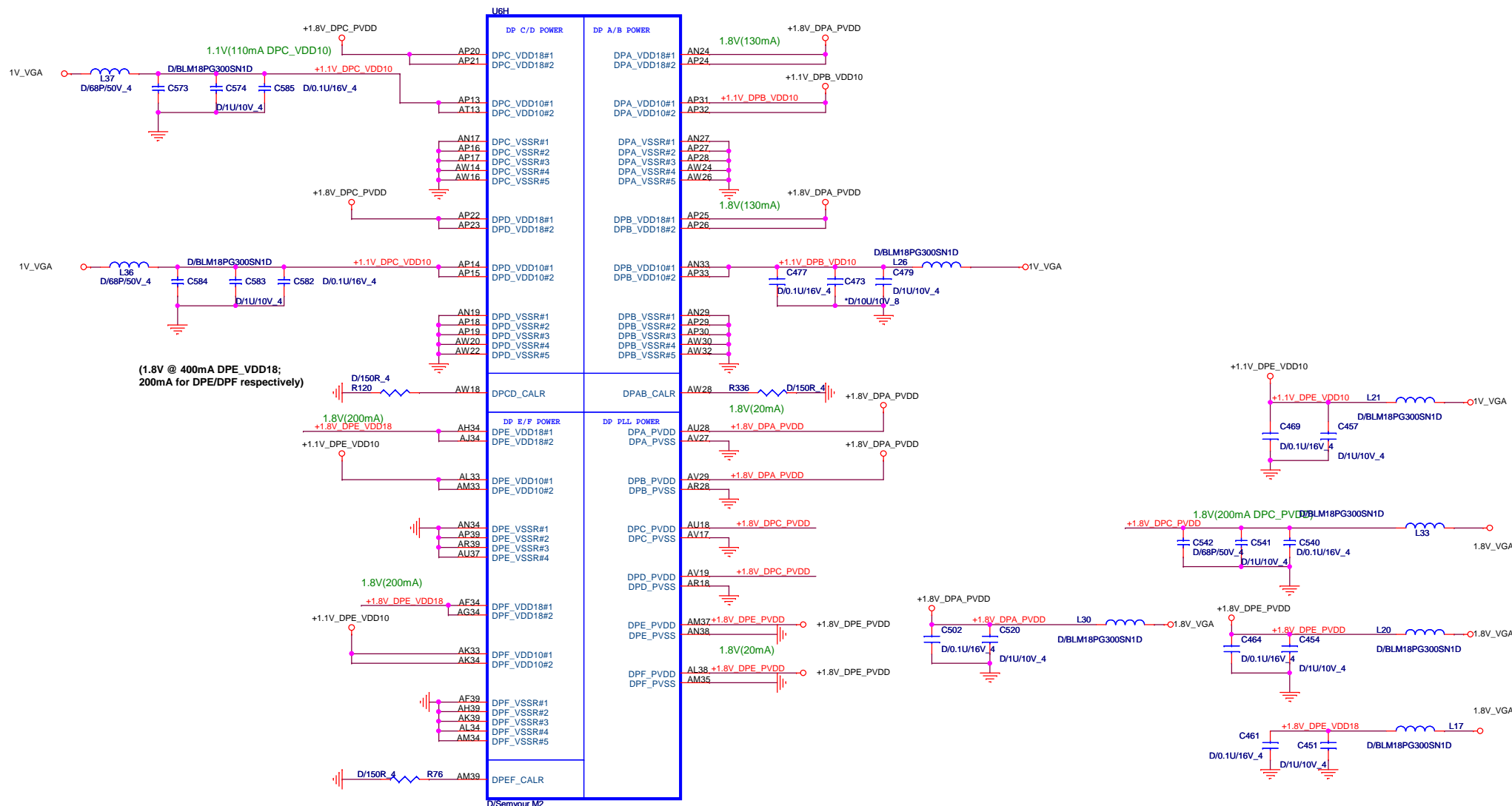


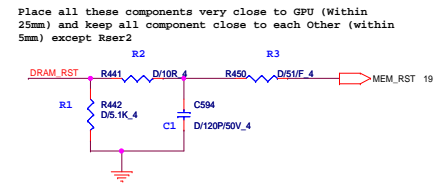
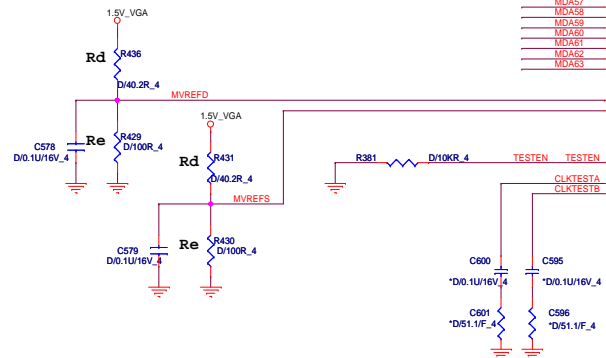
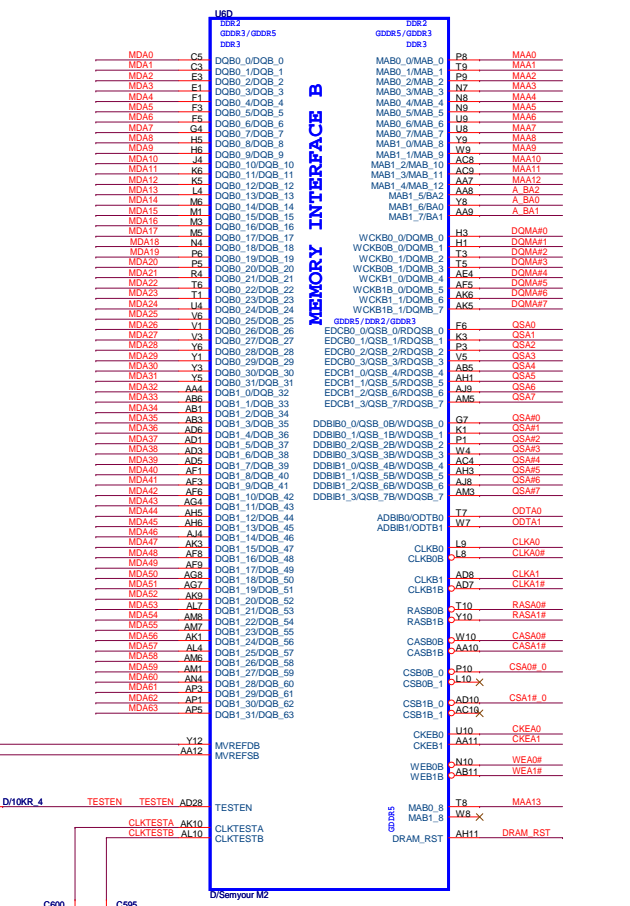
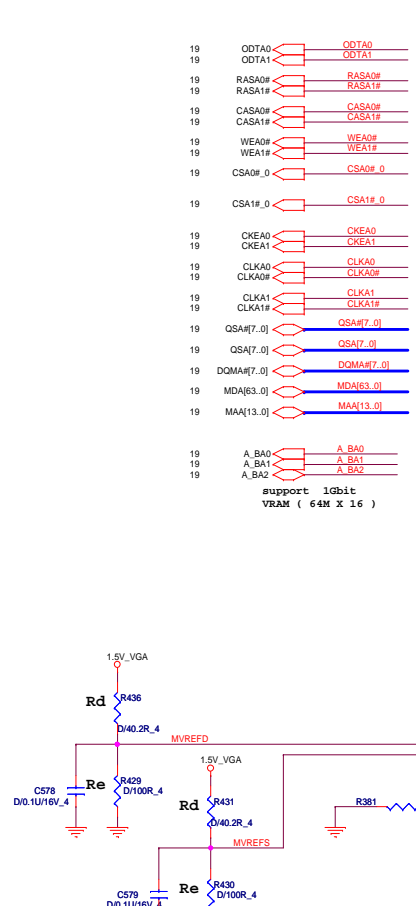
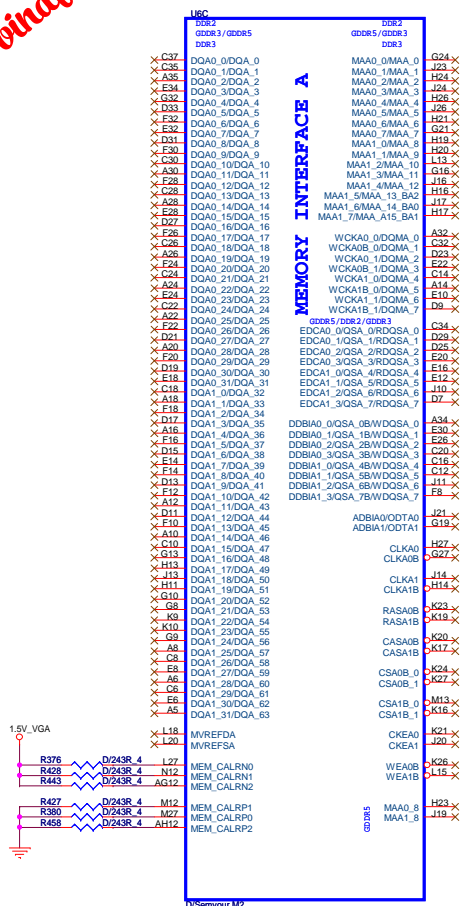


CNTRL1	CNTRL0	V-CORE
1	1	0.85V
1	0	0.9 V
0	1	1.0 V
0	0	1.1 V

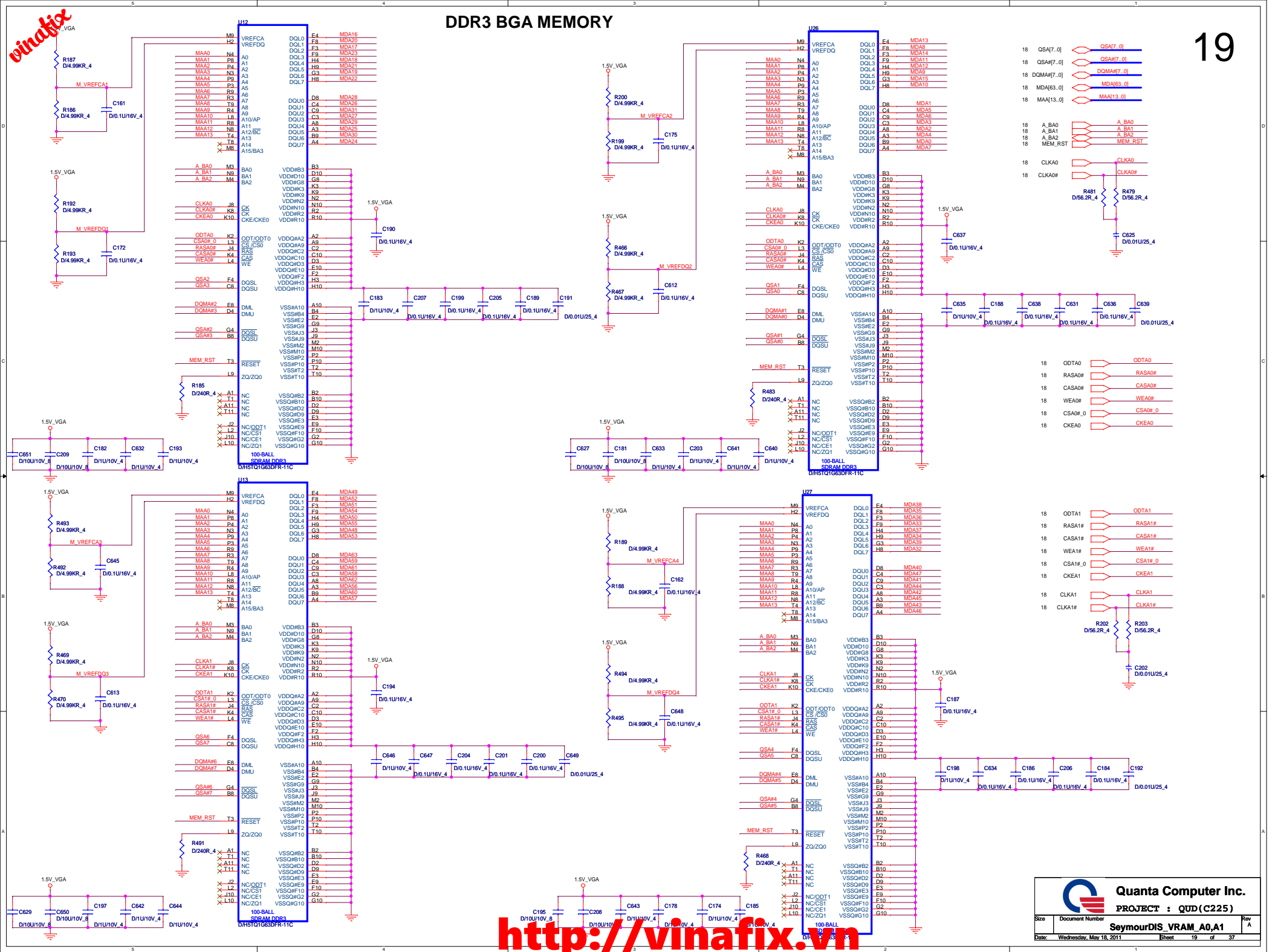


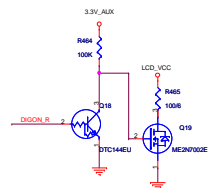




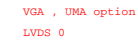


Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2

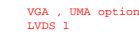




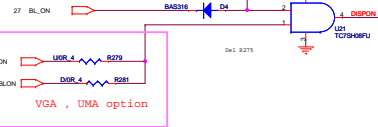
PANEL BACKLIGHT CONTROL



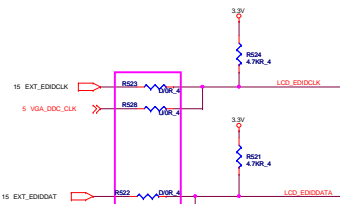
LVDS 0



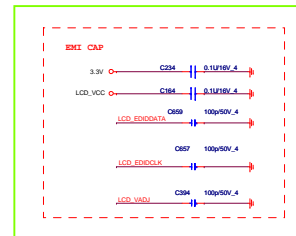
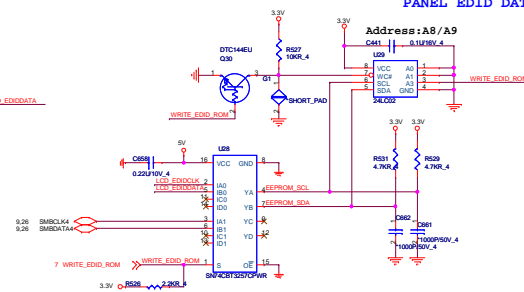
LVDS 1

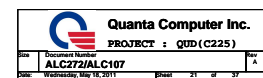


VGA , UMA option



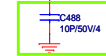
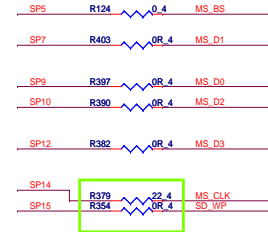
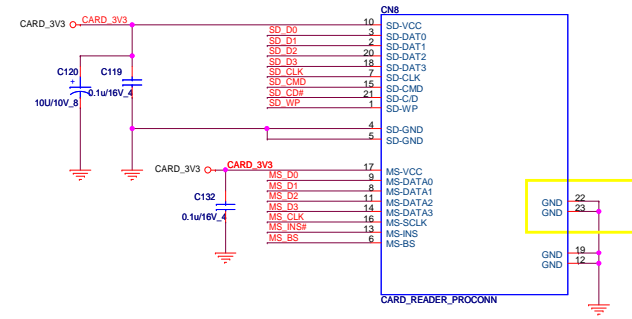
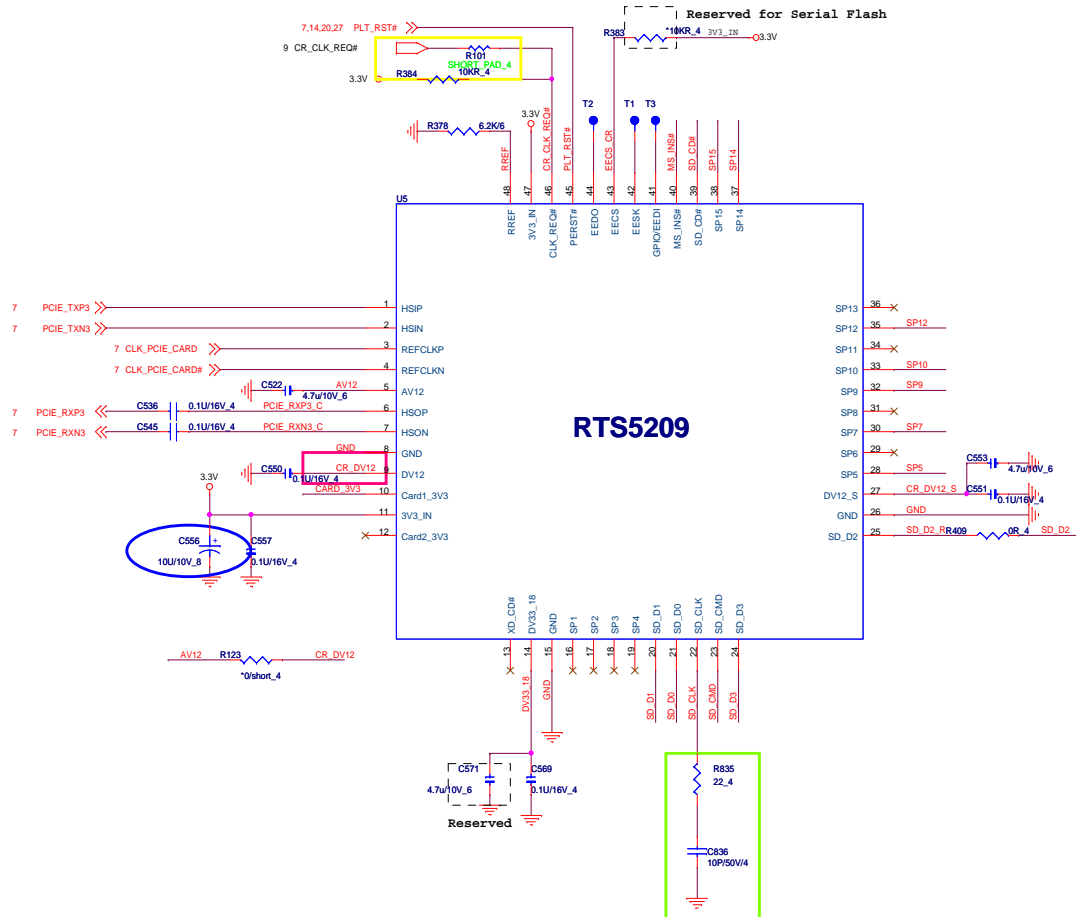
EEPROM IIC Selection





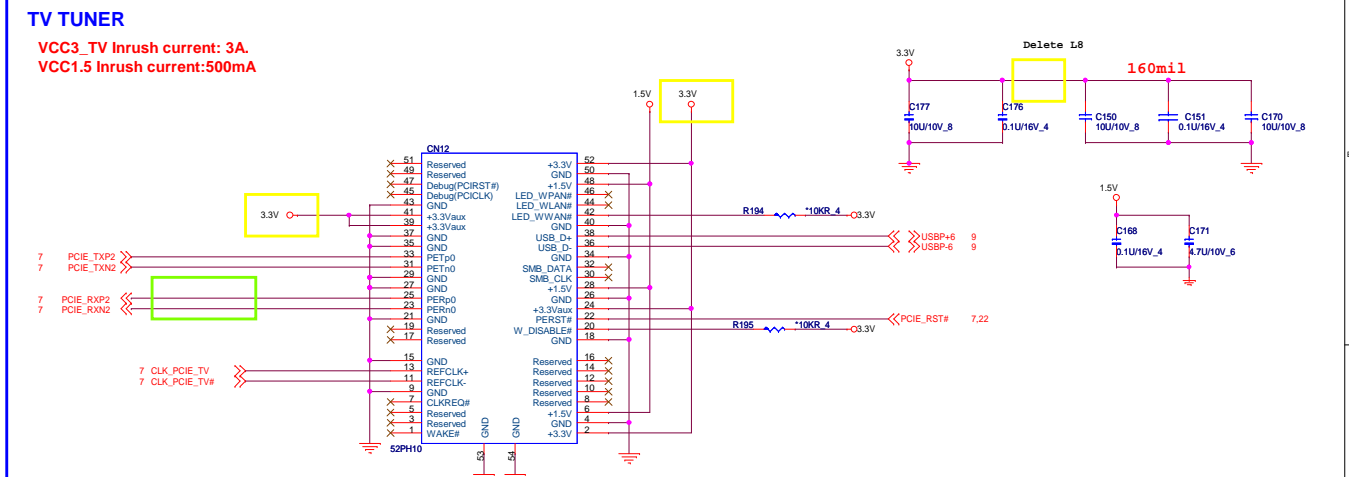
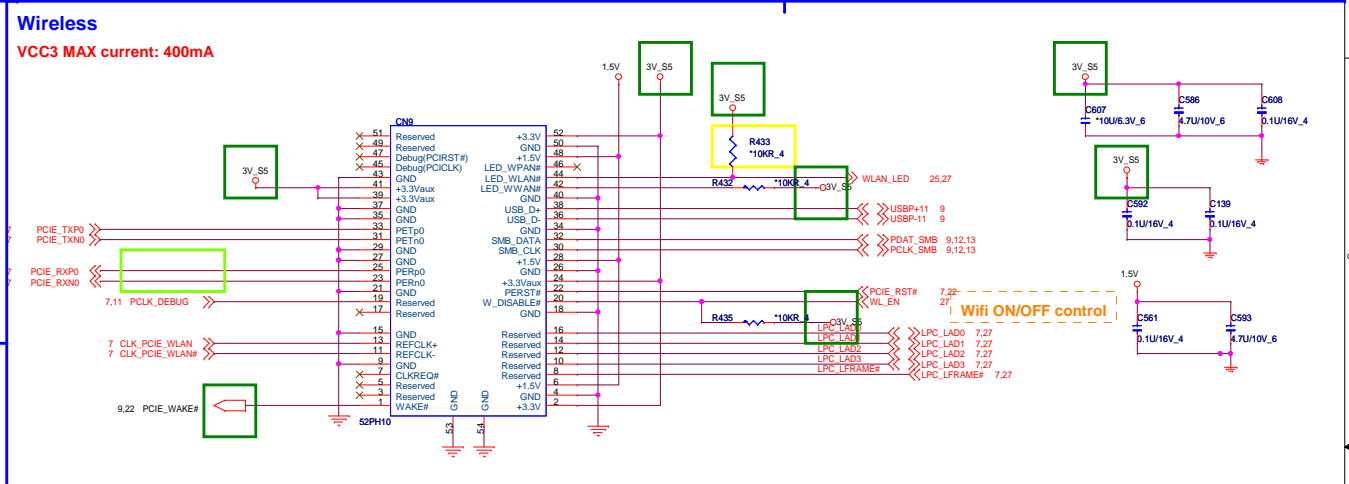
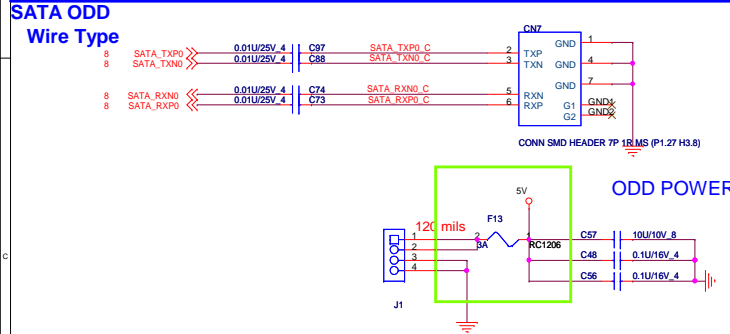
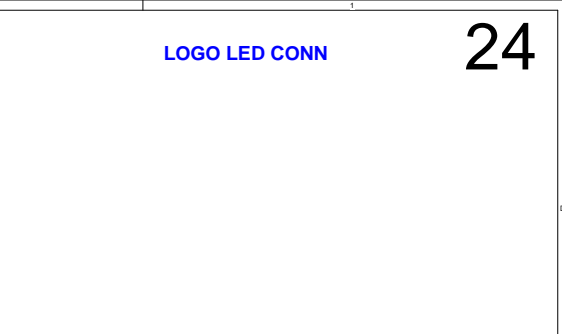
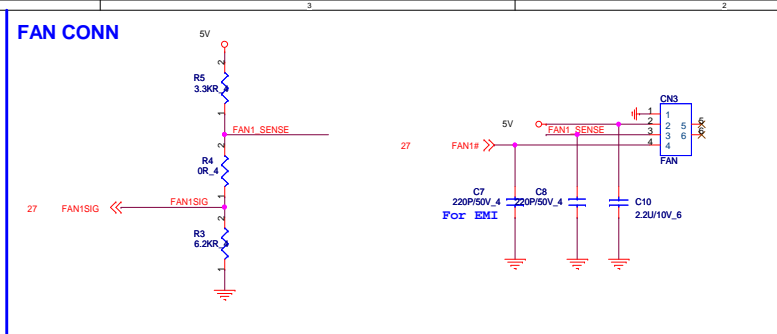
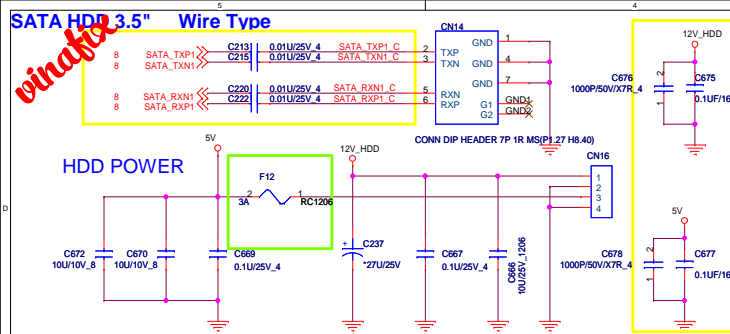
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4 IN 1 CARD READER



Share Pin

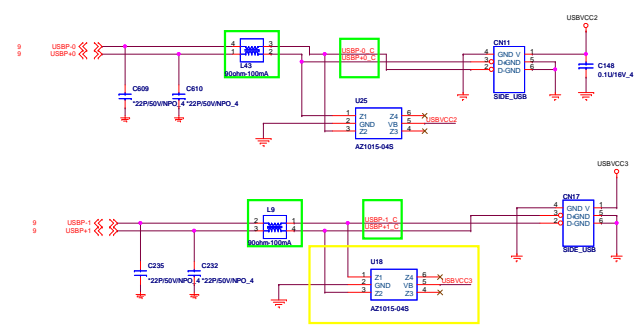
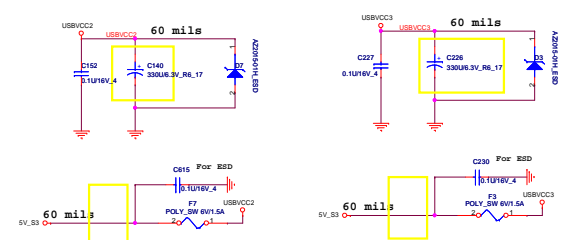
Share Pin	XD	MS	SD
SP1	XD0/B#		SD_D7
SP2	XD_RE#		SD_D6
SP3	XD_CE#		SD_D5
SP4	XD_WE#		SD_D4
SP5	XD_CLE	MS_BS	
SP6	XD_ALE	MS_D5	
SP7	XD_WP	MS_D1	
SP8	XD_D0	MS_D4	
SP9	XD_D1	MS_D0	
SP10	XD_D2	MS_D2	
SP11	XD_D3	MS_D6	
SP12	XD_D4	MS_D3	
SP13	XD_D5	MS_D7	
SP14	XD_D6	MS_CLK	
SP15	XD_D7		SD_WP



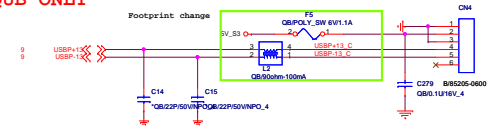
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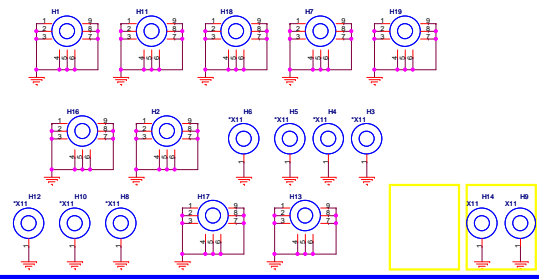
Side I/O USB X2



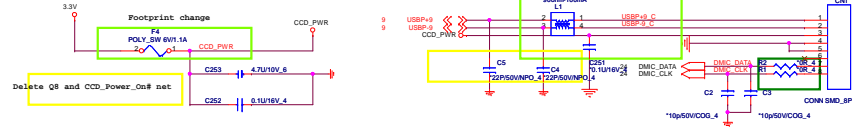
Touch Panel (Define by EETI module)
QUB ONLY



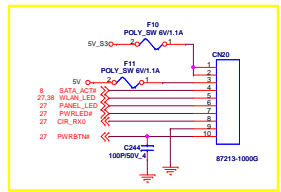
HOLE



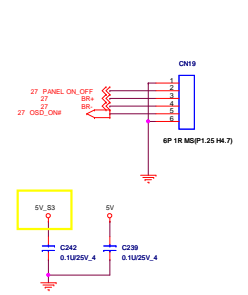
WEB CAM MODULE
(Define by Bison CCD module)



POWER SWITCH/LED

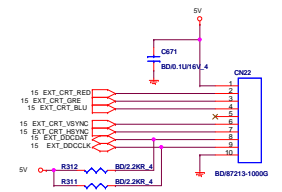


FUNCTION BUTTON BOARD

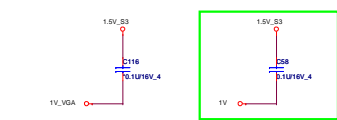
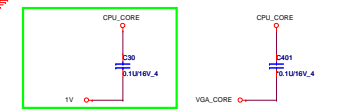
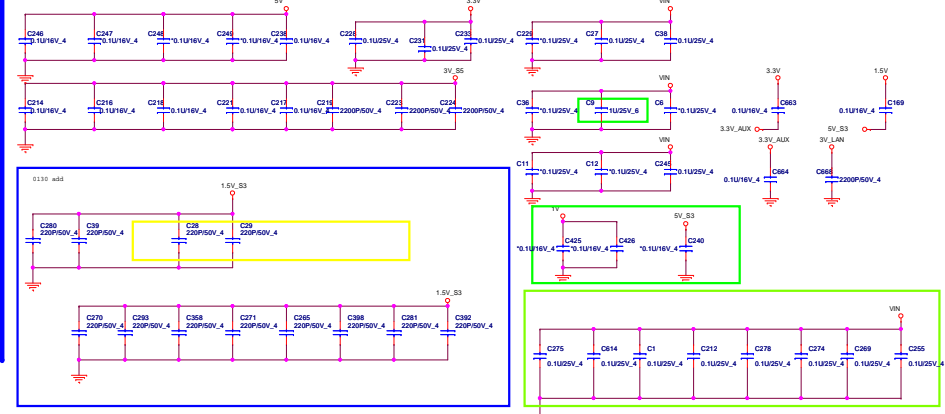


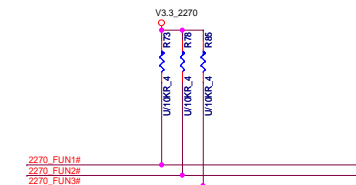
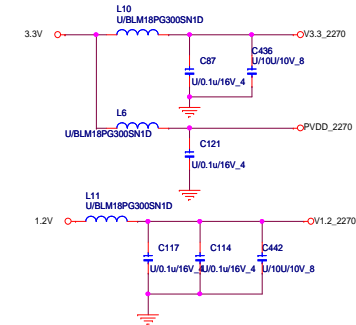
UMA CRT FOR DEBUG

Discrete CRT for Debug



EMI CAP

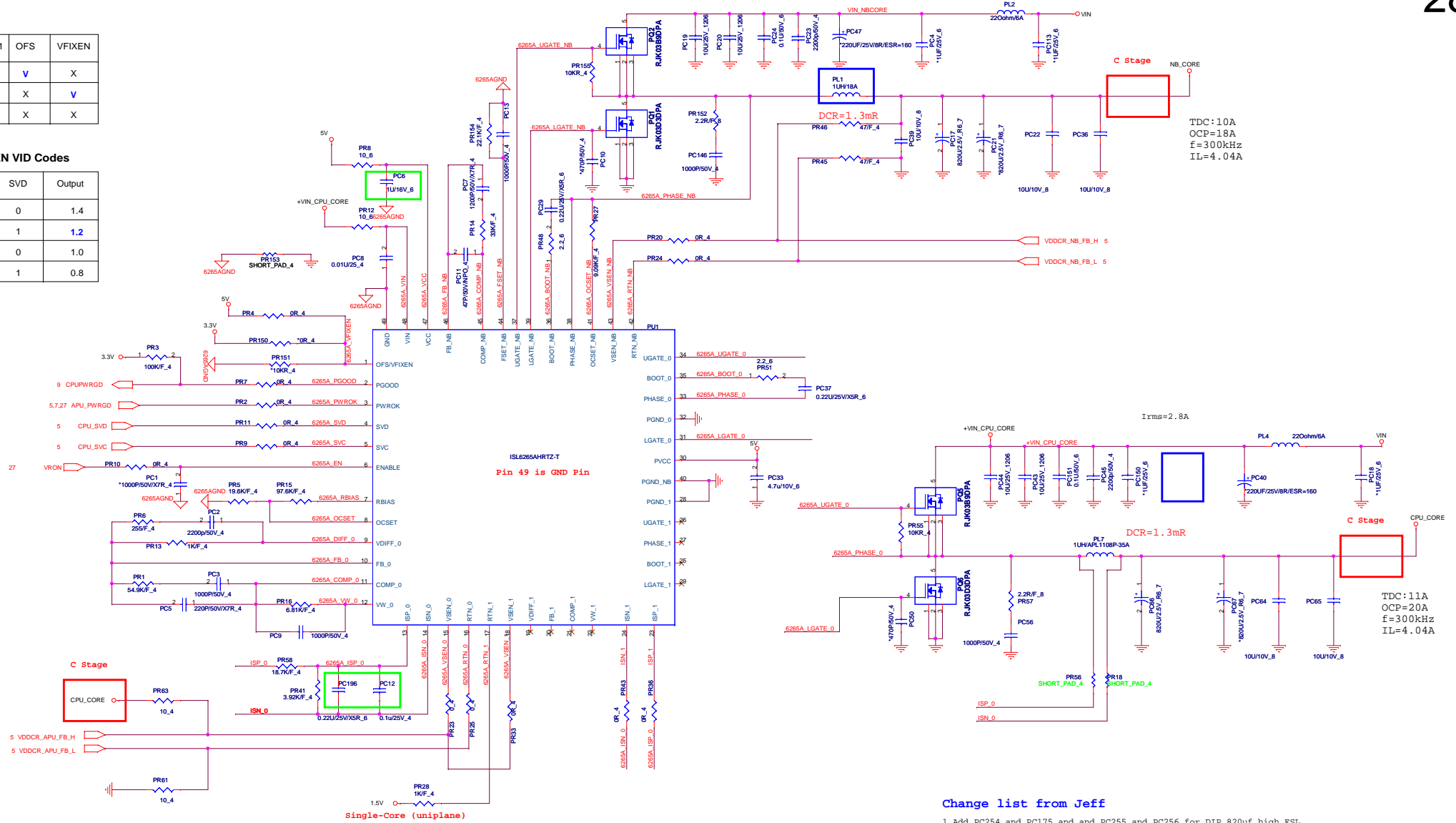




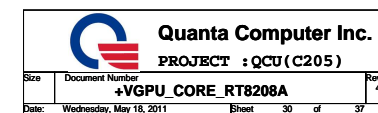
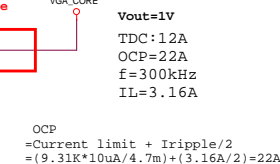
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

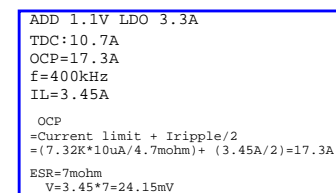
VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8





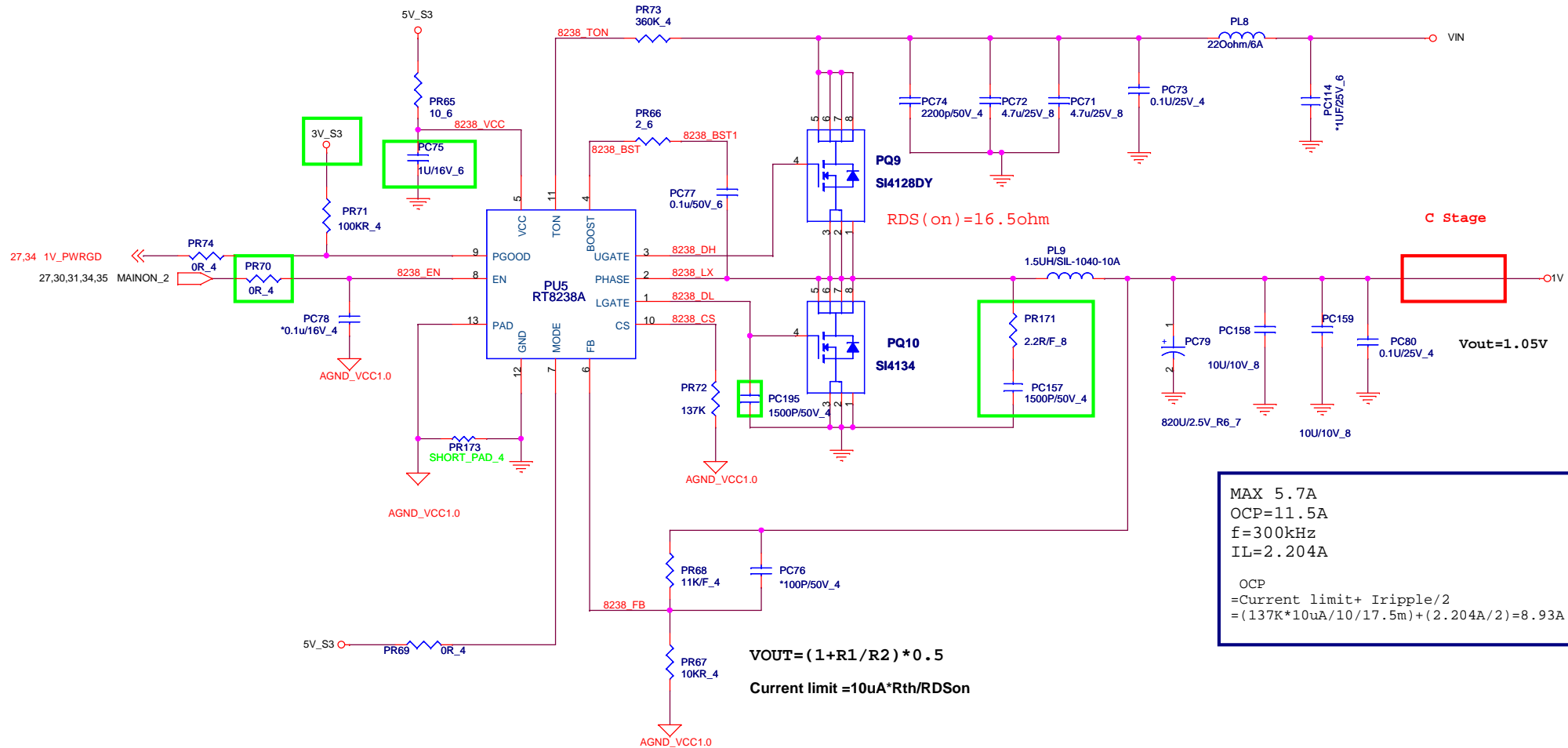




TDC:6.5A
OCP=12A
f=400kHz
IL=2.3A

ESR=16mohm
V=2.3*16=37mV

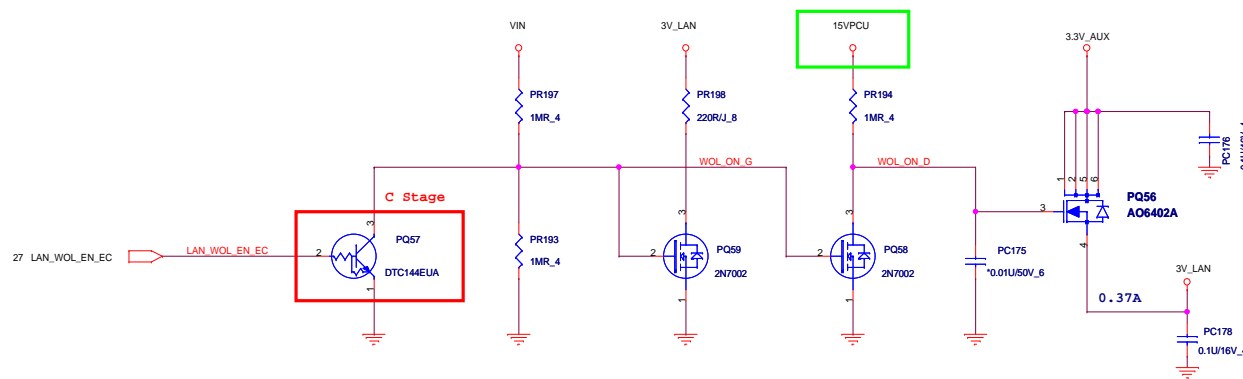
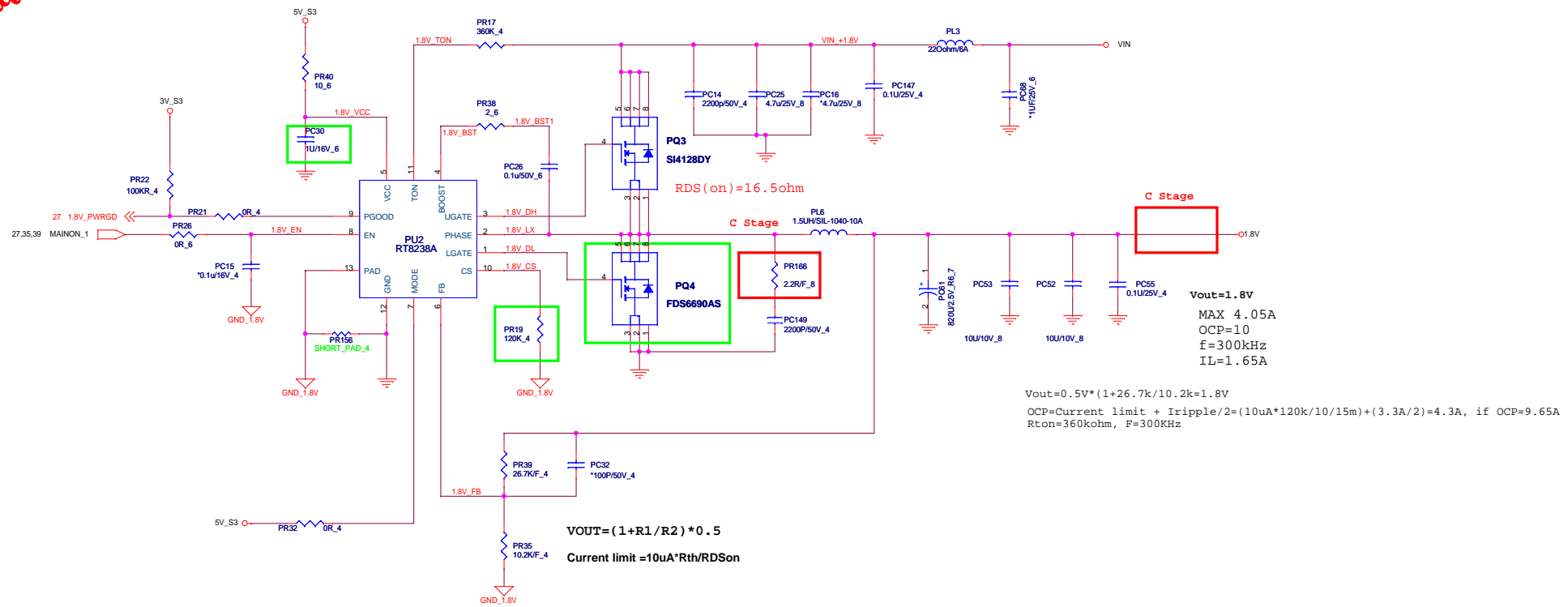
$$\begin{aligned} \text{OCP} &= \text{Current limit} + I_{\text{ripple}}/2 \\ &= (5.1\text{K} \cdot 10\mu\text{A} / 4.7\text{mohm}) + (2.3\text{A} / 2) = 12\text{A} \end{aligned}$$

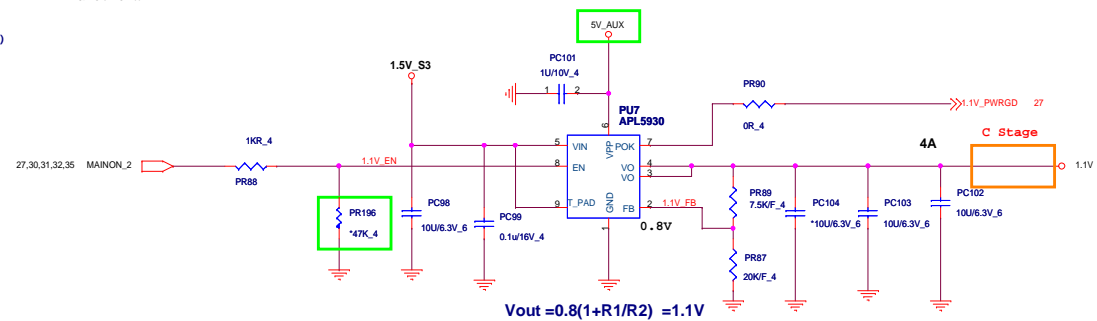
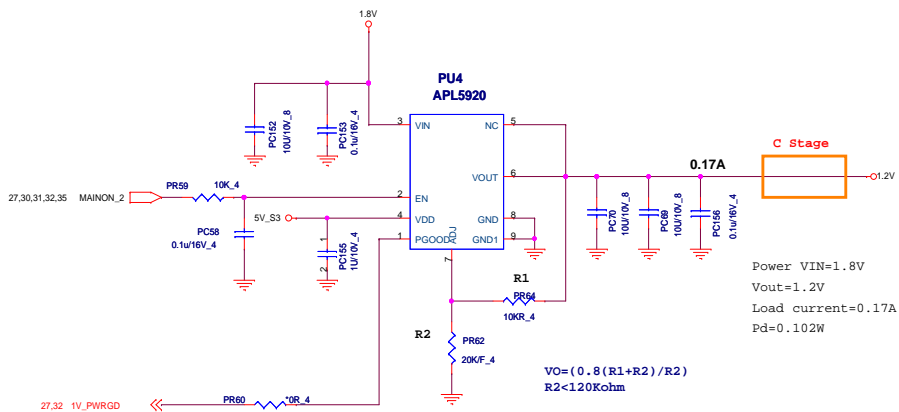
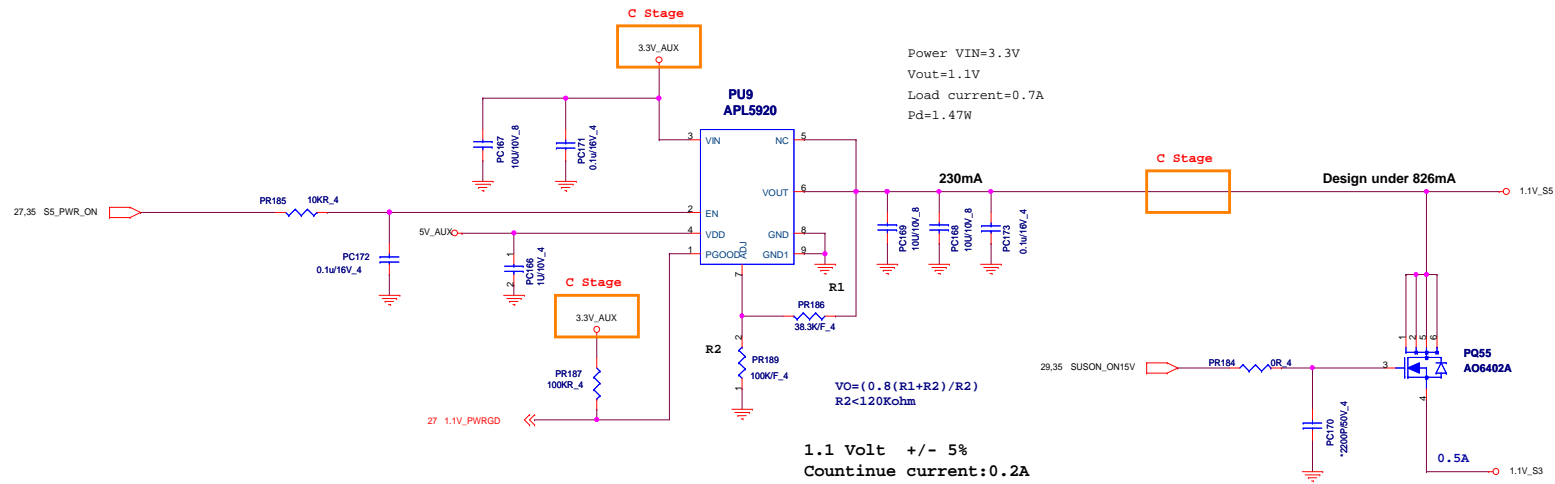


Quanta Computer Inc.

PROJECT : QCU (C205)

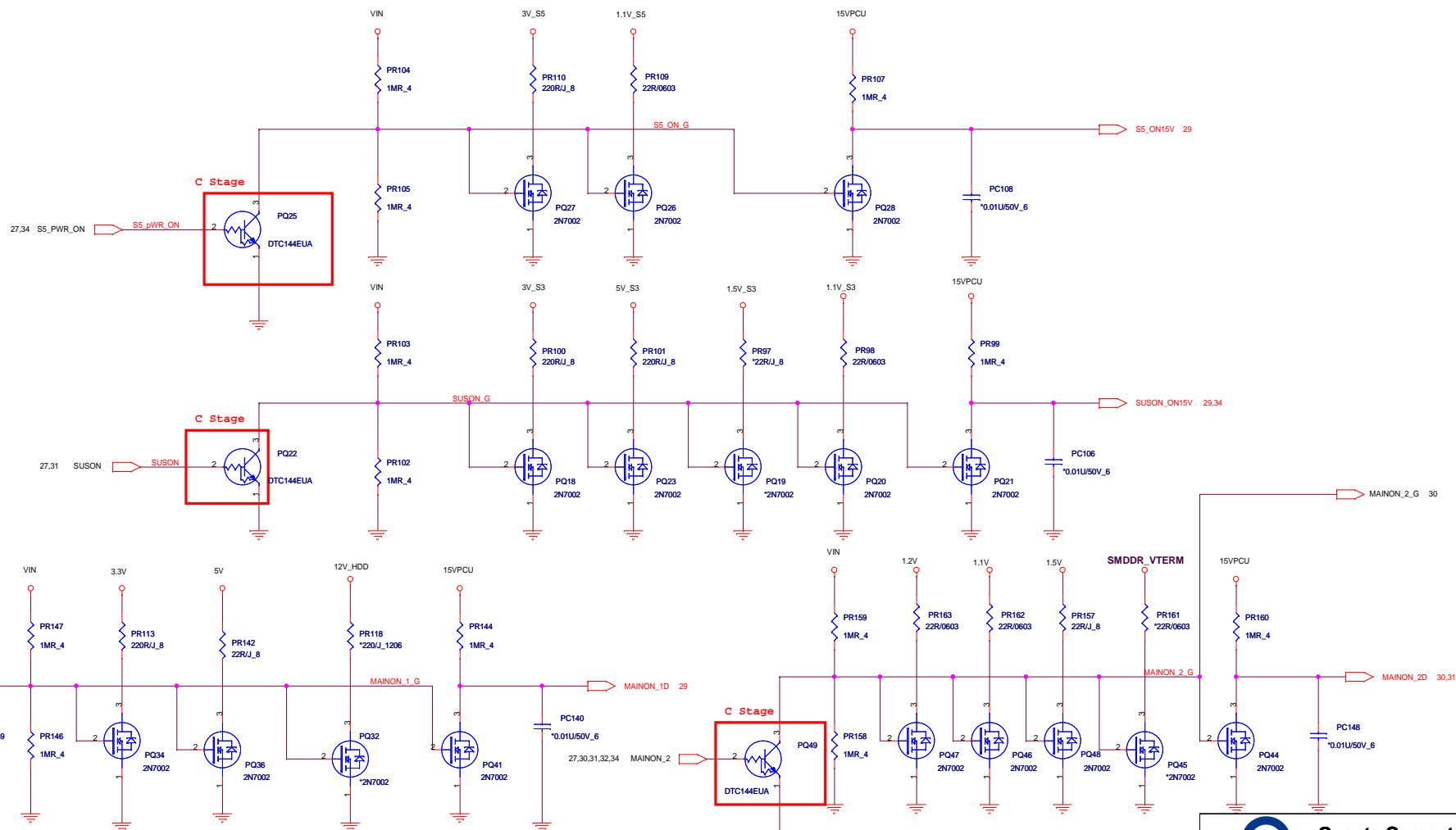
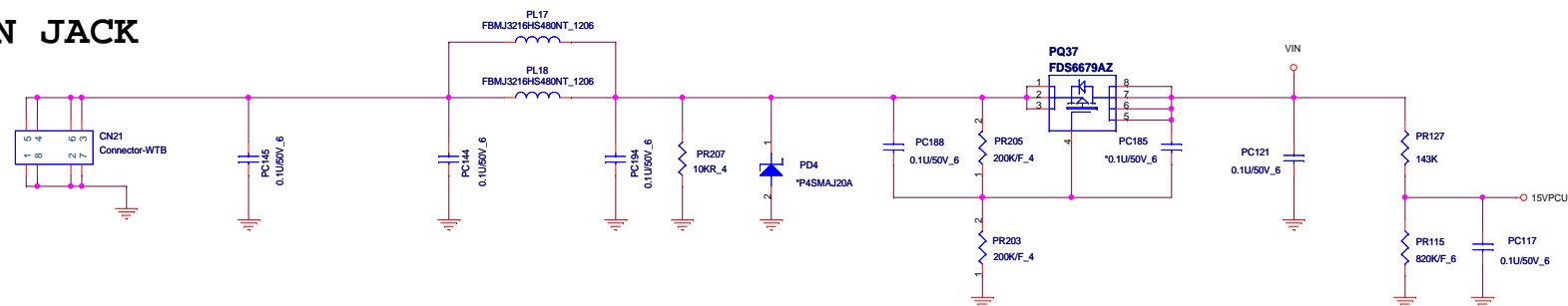
Size	Document Number	Rev
	VCC1.0(RT8202A)	4D
Date:	Wednesday, May 18, 2011	Sheet 32 of 37

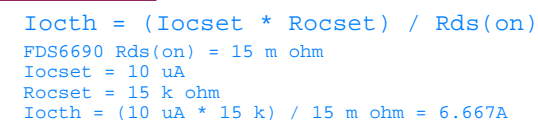




ramp-up time for all power rails
 50 us <All power rails except 5V_S5 <40 ms
 100 us <5V_S5<40 ms

DC IN JACK





1. Reserve R22,U23,C400,C365-For debug use.
2. Reserve R19 and Mount R18-Enable HDMI function.
3. Reserve R289,R290,R297,R302,R6.
4. Change power source change to 3.3V_LDO
5. Reserve/Short R184,R160,R337,R398,R321,R117,R389.
6. Delete L8 and Change 3.3V_TV power source to 3.3V
7. Add C3170,C3171,Y5,R808,R809,R8011,R8012,R8013.
8. Delete Q8 and CCD_Power_on# net
9. Reserve C5,C4.
10. Delete R434,R426,R423,R422,R415.
11. Delete LED1-LED6, Q9-Q13, R304-R309 for debug use.
12. Change C242 power source to 5V_S3.
13. Delete L7,C243,C225.
14. Change CN20 pin1 power to 5V_S3, pin 2 to VCC5 and delete pin8 CIR_RX0 net.
15. Add F10,F11 for safety concern.
16. Change C140,C226 footprint.
17. Del R172 not mount
18. Del R275 not mount
19. R7 from 150 ohm change to 499 ohm
20. MB_HDMI_DDCCLK change link to CN15[B18]
21. MB_HDMI_DDCDATA change link to CN15[B19]
22. Change CN7 footprint
23. Change J1 footprint
24. Change CN14 footprint
25. Change CN16 footprint
26. Change CN11,CN17 footprint
27. Change CON1, CON2 footprint

power 3/22

28. change PC87 to SMT type
29. PC138,PC184,PC116,PC149,PC134,PC190change to 2200PF
30. PR70 change to 0402 type
31. PR171,PR166 mount 2.2 ohm,PC151 1500PF
32. add PC19(1500pf)
33. add PC163(0.22uf)
33. PR135 change to 150K
34. PR116 change to 115K
35. FV7 pull low 47K.
36. delete PC100
37. PQ4,PQ40 change to FDS6690AS
38. PR19 change to 120K
39. PC96 change to 0603 type
40. FV7 pin6 change net to 3V_AUX
41. PR71 pull high change to 3V_S3
42. PC179 change to 0603 type
43. PC6,PC92,PC38,PC35,PC75,PC30 change to 0603 type

3/25 update

44. Add D26,D27,D28,D29 diodes
45. Change U18 AZ1015-048
46. CN18 add Pin 22, 23 link to GND
47. Change AR29 to 100K ohm
48. Change power net from AVDD to VREG5
49. Change Q6,Q7 add Q5523, Q5524 2N7002
50. 12V_HDD add C675,C676 for EMI
51. 5V add C677,C678 for EMI
52. CN14 change link [2]SATA_RXP1_C
53. CN14 change link [3]SATA_RXN1_C
54. CN14 change link [5]SATA_TXN1_C
55. CN14 change link [6]SATA_TXP1_C
3/28 update
56. Del APU_VADJ_2130S net, R288, R64,SW1, R69, R91 for Adj/MB
57. Del R8218, R79, FCH_14318M_CR net use external crystal for Scalar
58. Short pad R101
59. Reserve R433,
60. Change C226,C140 to 330U/6.3V_R6_17 SMD type
61. Change H1 footprint to hg-c276d138p2
62. Change R462 footprint to short0603.
63. Add R536, R537, R538, R539 reserved resister for EMI
64. Remove DDR window component. (C25, C26, C55, C33, C34)
65. Del H15 for DXF
3/29 update
66. D26,D27,D28,D29 change to 1S8355
67. Change R8011,R8012,R8013 to 75ohm
68. AR27 change to 100k ohm
69. Add CIR_RX0 net
70. CN21 change footprint for layout vicky
71. Add AR51 1K ohm for decrease current when power on.
72. Add R8014,R8015 and Q5525 for HDMI hot plug detect for Discrete SKU.

3/30 update

73. H13 change footprint
4/1
74. CN14 change link [2]SATA_TXP1_C
75. CN14 change link [3]SATA_TXN1_C
76. CN14 change link [5]SATA_RXN1_C
77. CN14 change link [6]SATA_RXP1_C
4/17
78. Change power net name FV9[3], PR187[1]from 3V_AUX to 3.3V_AUX
79. Modify DDR page need to mount the parts
4/27
80. Del USB_OC function, D28,R235,R236,PR108, USB_OC7#_R
81. Del USB_OC function, D29,R131,R132,PR182, USB_OC4#_R
82. Del USB_OC function, C673,F2,D26, R225,R220, PR181 USB_OC5#_R
83. Del USB_OC function, C674,F1,D27, R224,R219, PR183 USB_OC6#_R

5/08 update
84. Reserve DMICInterface R1,R2,C2,C3
85. R184 footprint change to Short0402
86. OSD_ON# add 4.7K ohm R810 pull up to 3.3V
87. EC Pin 69 2270_FUN1# move to EC pin 16
88. EC Pin 70 2270_FUN2# move to EC pin 120
89. EC Pin 71 2270_FUN3# move to EC pin 115
90. EC_PHYSICS (R490)and EC_WHITE(R487)3.3V_LDO power change to 3.3V
91. Reserve CON3
92. Reserve R480 WL_EN Pull up resister
93. WLAN change power from 3.3V change to 3V_S5
94. Add audio bias voltage AR65.AR66,AR67,AR68,AR69, AR70,AC49,AC50

5/11 update Jeff

84. PR166 chang to 0805 type
85. PLL14 change PN which vendor TTY
86. PC87 change to 330uF and add PC197
87. PQ22,PQ25,PQ39,PQ49, PQ57 change PW
88. Delete PR164,PR167,PR174,PR145,PR168,PR169,PR172,PR198,PR191,PR79,PR91
5/11 Anson
89. CN9 Pin1 lin to PCIE_WAKE#
90. R435 change to 3V_S5
91. R432 change to 3V_S5
92. R536,R537,R538,R539 change to 150 ohm
93. R6 remove to BOM(short pad)
94. EC pin 73 link to R811,R812

R0C-->R0D

6/09

95. Del U8 TC7SH08FU
96. Add fuse at HDD/ODD 5V power for 3C test
97. Modify NUT P/N to MBQU1002010 for H9, H14 location
98. Add U34,U35 EEPROM Co-lay

power 6/15

99. PC127 change to 330p
100. PC126 change to 0.022uf
101. PC125 change to 8200pf

6/17

102. CN7 change footprint to sata-ld1107f-s33t5-7p-r